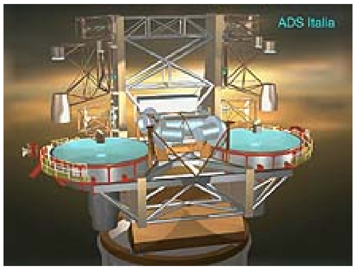

LBT PROJECT

2 x 8.4m OPTICAL TELESCOPE

Instrument Rotator and Cable Chain Application Board Description and Operations Manual

	Signature	Date
Prepared	J. Rosato	12-Mar-07
Reviewed	D. Ashby	19-Mar-07
Approved		

1. Revision History

Issue	Date	Changes	Responsible
a	12-Mar-07	First draft	J. Rosato

2. Table Of Contents

3. About this document

3.1. Purpose

This document describes the **Instrument Rotator and Cable Chain Application board (IRCCAB)**. This document is intended as an operator's manual as well as a technical description of the module.

A description of how this product is interconnected with the Drive Power Module and to encoders on the rotators is provided.

Technical information such as bill of materials, schematics and printed circuit board layouts for use in maintaining and debugging the IRCCA to the component level are listed among the Reference Documents.

3.2. Reference Documents

[RD1] CAN Document 670s007a – Instrument Rotator and Cable Chain Detailed Design Description.

[RD2] CAN Document 675s001a – General Purpose SERDES Communications Protocol Standard

[RD3] CAN Document 675s002a – General Purpose SERDES Communications PC Board Description and Operations Manual

[RD4] CAN Document 675s003a – Instrument Rotator and Cable Chain Reef SERDES Interface Module Description and Operations Manual

[RD5] CAN Document 675s004a – Instrument Rotator and Cable Chain Interface Module Description and Operations Manual

[RD6] CVS Document TBD, Rotator Application Board VHDL code

[RD7] CVS Document TBD, Rotator Application Board Embedded Processor code

3.3. Abbreviations

MCS – Mount Control System
MCSPU - Mount Control System Processing Unit
FPGA – Field Programmable Gate Array
SERDES – Serializer - Deserializer
CRC - Cyclic Redundancy Check
VHDL- Very High Speed Integrated Circuit Hardware Description Language
DGR - Direct Gregorian Rotator
BGR - Bent Gregorian Rotator
TBD - To Be Determined
DAC – Digital to Analog Converter
ADC – Analog to Digital Converter
mA - Milliamps

4. Instrument Rotator and Cable Chain Application Board Overview

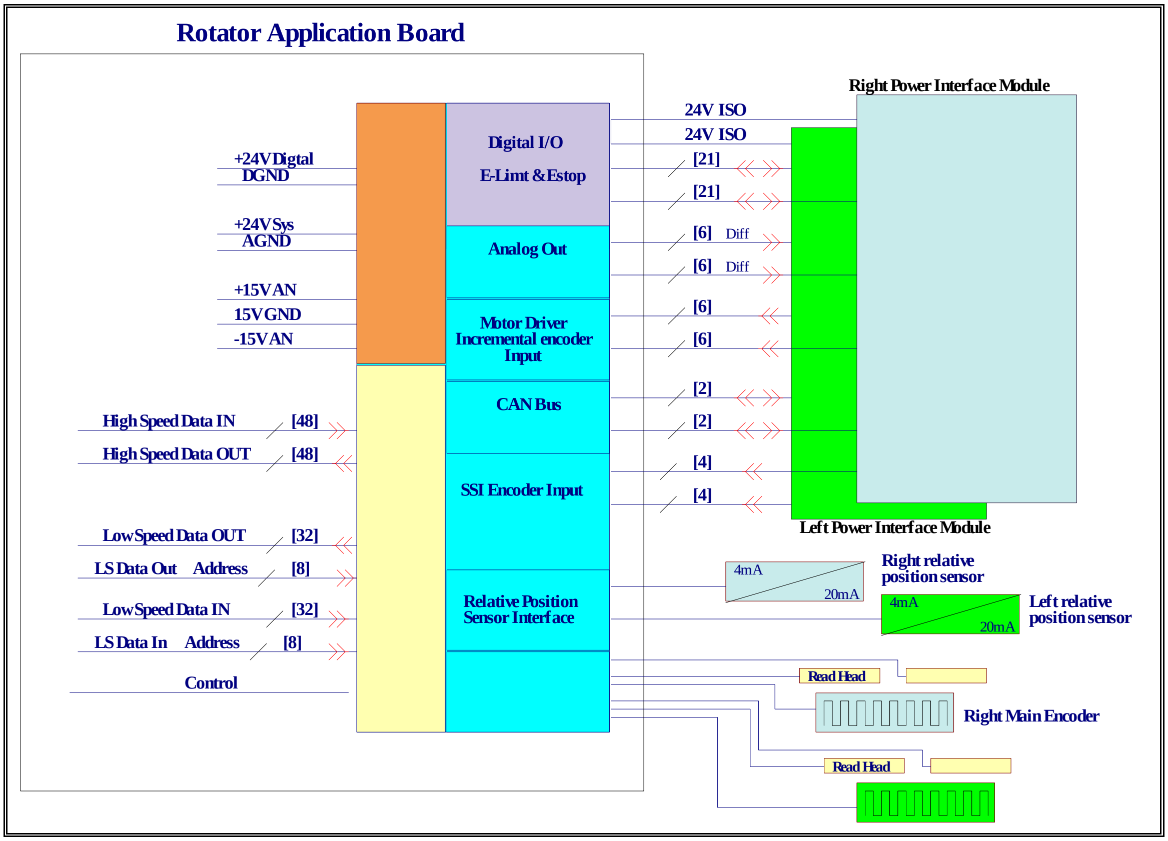

Figure 4.0.1: Block Diagram of the IRCCAB

Figure 4.0.1 shows a block diagram of the Instrument Rotator and Cable Chain Application board interfacing to the Rotator subsystems.

The General Purpose SERDES Communications Board (GPSCOM) [RD2] receives frames of data from the Instrument Rotator and Cable Chain Reef SERDES Interface Module [RD4] located in the Aux Control Room. This data is then de-serialized on the GPSCOM Board and it produces a parallel interface for the Instrument Rotator Applications board. As shown in **Figure 4.0.1**, this interface consists of a 48-bit High-Speed Data In bus and 8-bit High-Speed Data Out bus, a 32-bit Low-Speed Data Out bus, a 32-bit Low-Speed Data In bus, an 8 bit address bus and a control bus. See **Figure 4.1.1** for more details.

4.1. Instrument Rotator Application Board

The following sections give a functional overview of each of the Instrument Rotator Application Board sections. Refer to back figure 4.0.1 for a block diagram of these sections.

For more detail on how these are used in the rotator system, see [RD5].

4.1.1. Power Requirements

The Instrument Rotator Application board requires 4 separate voltages. Table 4.2.1 below details these power supply requirements.

Power Input	24 Volt Digital ISO Supply @ TBD mA
	24 Volt Analog Voltage @ TBD mA
	+15V Analog @ TBD mA
	-15V Analog @ TBD mA

Table 4.2.1

4.1.2. Digital I/O section

The Instrument Rotator Application board provides optically isolated digital I/O used to interface with two Rotator Power Interface Modules. All power for this interface is provided by a separate 24 Volt power supply (24 Volt Digital ISO Supply) which allows isolating the motor drive analog functions from the digital functions and provides a separate grounding systems with a single point ground at the rack mount power supply output.

4.1.3. Analog outputs

The Instrument Rotator Application board provides 12 16-Bit DAC outputs through differential drivers.

These signals are torque commands for the drives. The actual voltage seen by the drives on each of their corresponding analog inputs is available through the drive's CAN bus interface.

These signals are differential and use AGND as a reference.

4.1.4. Motor Driver Incremental Quad Encoder Interface

The Instrument Rotator Application board receives incremental encoder signals produced by the motor drivers. These signals are RS422 differential signals.

The Application board provides the necessary interface to provide the system software with rate information from these signals. This information is produced by the logic inside the FPGA.

4.1.5. CAN Bus

The Instrument Rotator Application board provides a CAN bus interface to two separate Rotator Power Interface Modules. The signals are driven out two separate connectors to minimize the possibility of producing a ground loop between the Rotator Power Interface Modules and the Instrument Rotator and Cable Chain Interface Module.

The CAN bus interface is provided by an 8051 microprocessor running the CAN open communications protocol [RD9]. The CAN bus provides almost all the information regarding the status of the drives. Motor current, bus voltage, and drive ambient temperature are a few of the system parameters available and provided by the CAN interface. See [RD1] for information regarding the status information returned for each drive from the CAN bus interface.

The 8051 program queries the 6 motor drivers connected to its CAN bus for specific dive status. Once it has obtained this data, it writes it to specific memory locations in the FPGA, which are mapped into the 8051 I/O space. This information is mapped through the FPGA on board to the GPSCOM Low-Speed bus. The System software can then access this information. See [RD1] for information regarding the status information returned for each drive from the CAN bus interface.

4.1.6. Relative Position Sensor Interface

The Instrument Rotator Application board interfaces two separate linear position sensors. These sensors provide information about the relative position of the cable chain and rotator. The Rotator Application board provides power (24VDC) and a reference (AGND) for the sensors. The sensors output a 4-20mA signal proportional to the relative position of the cable chain to the rotators. The interface circuitry for this signal measures the output current and provides an output voltage proportional to the current. The circuitry also detects when no current is present in order to indicate a problem with the sensor or with field wiring.

4.1.7. Inductosyn Tape Interface

The Instrument Rotator Application board interfaces to two Inductosyn tape encoders and four tape heads. For both the left and right rotators, the board provides power for the head preamps, signals to excite the tapes and interface circuitry to interpolate the signals from two separate heads which measure position for each.

The signals from the heads are amplified by a preamp located close to the heads. The preamp system outputs differential sine and cosine signals.

The Application board provides interface circuitry that will produce a single ended sine and cosine signal. These signals can then be input to a resolver to digital converter IC such as the AD2S81A. The AD2S81A is capable of producing a 16-bit digital result proportional to tape head position.

Additionally, rate (tack) information is available from this interface.

4.1.8. SSI Encoder Interface

The Instrument Rotator Application board interfaces with four SSI absolute position encoder subsystems (2 on the left and 2 on the right).

The interface provides 24 Volt power and a differential clock signal for each encoder. The encoders provide differential data in response to the clock signals from the application board.

The hardware interface is RS422 (Differential).

5. FPGA and 8051 Processor

An FPGA and an 8051 type processor provide the interface and logic resources on the Application Board.

The FPGA is a SRAM based Xilinx Virtex II 500,000 logic gate device in a 456 pin ball grid array (BGA) package. Configuration of the FPGA is done via a JTAG interface. The JTAG chain can be configured to support the local FPGA and Xilinx XC18V04 configuration PROM. The JTAG chain looped through the GPSCOM board to the application board. This configuration allows a single JTAG port to support both boards when in their final configuration. A local JTAG port for configuring and debugging the Application in a stand-alone configuration is also provided.

The FPGA firmware for the rotator is a synchronous design written in VHDL [RD6]. The final configuration code is stored in a Xilinx XC18V04 configuration PROM on the board. The board is automatically configured on power-up or by depressing the program switch located on the board.

The FPGA contains modules to interface with the GPSCOM, SSI encoders, the 8051, DACS, quad encoders, Inductosyn subsystems, and motor driver digital I/O.

The 8051 is a System on Chip type devices containing on board Flash for the embedded system code [RD 7] as well as on board RAM.

The 8051 also contains a CAN bus hardware interface as well as a 12-bit ADC for monitoring system functions such as applications board voltages and temperature.

6. Mechanical Packaging and Environment

6.1. Environmental Specifications

Temp	0º to +50 ºC
Humidity	0 to 90% Non Condensing
Ventilation requirements	Unit must be mounted so that internal fans can draw air from one side of the module and exhaust air out the other side
Altitude	Operational to 11,000 ft
Power Input	24 Volt Digital Isolation @ 500 mA Max
	24 Volt Analog Voltage @ 1A Max
	+15V Analog @ 500 mA
	-15V Analog @ 500 mA

6.2. Mechanical Renderings

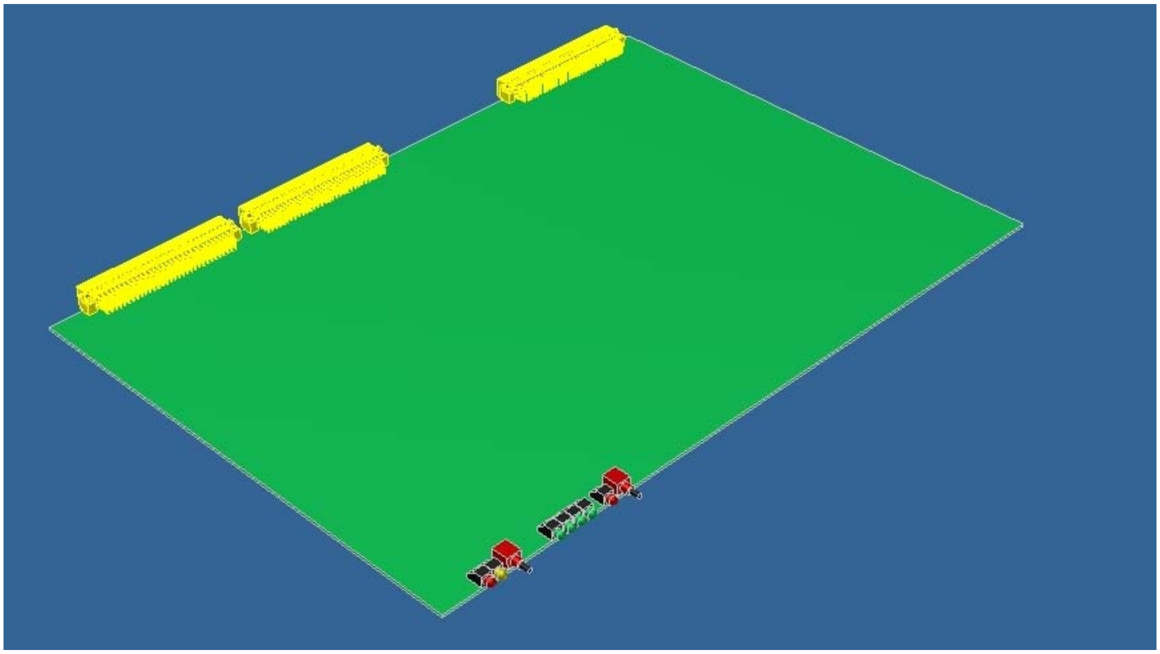

Figure 5.3.1: Isometric Rendering of Rotator Interface Board

7. Input and Output Specifications

The Application Board mates with two other PC boards, the (System Application Connector Board) SACB, and the GPCOM Board. All I/O for the Application Board occurs through these two interfaces.

7.1. GPCOM Board Interface

As Figure 4.0.1 shows, the GPCOM provides and interface with 2 high-speed busses (in and out) and 2 low-speed busses, as well as 7-bit address busses for both low- speed busses.

The GPCOM board also provides a clock signals and several control and status signals. The Applications Board uses the clock from the GPCOM board to synchronize all data flowing through the system.

The Applications board provides 24VDC power for the GPCOM board.

Two 120-pin high-speed connectors provide the physical interface for all these signals. The GPCOM board provides all I/O as single ended LVTTL signals. However; the FPGA can be programmed to provide different interface standards if needed.

Table 1 and table 2 below lists the signal and pin assignments on the two 120 pin high-speed connectors.

J3 Connector

Pin	Pin Name	Description
1	NC	No Connect
2	HS_IN(8)	High Speed Bus Input
3	NC	No Connect
4	HS_OUT(32)	High Speed Bus Output
5	ASYNC_RESET_OUT	Async reset Output
6	WDI/	Watchdog Timer Output
7	NC	No Connect
8	WR_EN	Low Speed Bus Write Strobe
9	NC	No Connect
10	HS_OUT(36)	High Speed Bus Output
11	SPARE_IN(0)	Spare I/O (to analyzer header also)
12	SPARE_IN(1)	Spare I/O (to analyzer header also)
13	SPARE_IN(2)	Spare I/O (to analyzer header also)
14	SPARE_IN(3)	Spare I/O (to analyzer header also)

15	SPARE_IN(4)	Spare I/O (to analyzer header also)
16	SPARE_IN(5)	Spare I/O (to analyzer header also)
17	SPARE_IN(6)	Spare I/O (to analyzer header also)
18	SPARE_IN(7)	Spare I/O (to analyzer header also)
19	SPARE_IN(8)	Spare I/O (to analyzer header also)
20	SPARE_IN(9)	Spare I/O (to analyzer header also)
21	SPARE_IN(10)	Spare I/O (to analyzer header also)
22	SPARE_IN(11)	Spare I/O (to analyzer header also)
23	SPARE_IN(12)	Spare I/O (to analyzer header also)
24	SPARE_IN(13)	Spare I/O (to analyzer header also)
25	SPARE_IN(14)	Spare I/O (to analyzer header also)
26	SPARE_IN(15)	Spare I/O (to analyzer header also)
27	NC	No Connect
28	NC	No Connect
29	HS_IN(37)	High Speed Bus Input
30	HS_IN(47)	High Speed Bus Input
31	HS_IN(45)	High Speed Bus Input
32	HS_IN(46)	High Speed Bus Input
33	TMS	JTAG TMS
34	TCK	JTAG TCK
35	TDI_APP	JTAG TDI
36	TDO_APP	JTAG TDO
37	HS_IN(43)	High Speed Bus Input
38	HS_IN(44)	High Speed Bus Input
39	HS_IN(41)	High Speed Bus Input
40	NC	No Connect
41	HS_IN(39)	High Speed Bus Input
42	HS_IN(40)	High Speed Bus Input
43	NC	No Connect
44	HS_IN(38)	High Speed Bus Input
45	NC	No Connect
46	HS_IN(36)	High Speed Bus Input
47	IN_ADDR(0)	Low Speed Input Bus Address
48	IN_ADDR(1)	Low Speed Input Bus Address
49	IN_ADDR(2)	Low Speed Input Bus Address
50	IN_ADDR(3)	Low Speed Input Bus Address
51	IN_ADDR(4)	Low Speed Input Bus Address
52	IN_ADDR(5)	Low Speed Input Bus Address
53	IN_ADDR(6)	Low Speed Input Bus Address
54	IN_ADDR(7)	Low Speed Input Bus Address
55	IN_DATA(0)	Low Speed Input Bus Data
56	IN_DATA(1)	Low Speed Input Bus Data

57	IN_DATA(2)	Low Speed Input Bus Data
58	IN_DATA(3)	Low Speed Input Bus Data
59	IN_DATA(4)	Low Speed Input Bus Data
60	IN_DATA(5)	Low Speed Input Bus Data
61	IN_DATA(6)	Low Speed Input Bus Data
62	IN_DATA(7)	Low Speed Input Bus Data
63	OUT_DATA(8)	Low Speed Output Bus Data
64	OUT_DATA(9)	Low Speed Output Bus Data
65	OUT_DATA(10)	Low Speed Output Bus Data
66	OUT_DATA(11)	Low Speed Output Bus Data
67	OUT_DATA(12)	Low Speed Output Bus Data
68	OUT_DATA(13)	Low Speed Output Bus Data
69	OUT_DATA(14)	Low Speed Output Bus Data
70	OUT_DATA(15)	Low Speed Output Bus Data
71	OUT_DATA(16)	Low Speed Output Bus Data
72	OUT_DATA(17)	Low Speed Output Bus Data
73	OUT_DATA(18)	Low Speed Output Bus Data
74	OUT_DATA(19)	Low Speed Output Bus Data
75	OUT_DATA(20)	Low Speed Output Bus Data
76	OUT_DATA(21)	Low Speed Output Bus Data
77	OUT_DATA(22)	Low Speed Output Bus Data
78	OUT_DATA(23)	Low Speed Output Bus Data
79	OUT_DATA(24)	Low Speed Output Bus Data
80	OUT_DATA(25)	Low Speed Output Bus Data
81	OUT_DATA(26)	Low Speed Output Bus Data
82	OUT_DATA(27)	Low Speed Output Bus Data
83	OUT_DATA(28)	Low Speed Output Bus Data
84	OUT_DATA(29)	Low Speed Output Bus Data
85	OUT_DATA(30)	Low Speed Output Bus Data
86	OUT_DATA(31)	Low Speed Output Bus Data
87	HS_IN(33)	High Speed Bus Input
88	HS_IN34)	High Speed Bus Input
89	HS_OUT(0)	High Speed Bus Output
90	HS_OUT(1)	High Speed Bus Output
91	HS_OUT(2)	High Speed Bus Output
92	HS_OUT(3)	High Speed Bus Output
93	HS_OUT(4)	High Speed Bus Output
94	HS_OUT(5)	High Speed Bus Output
95	HS_OUT(6)	High Speed Bus Output
96	HS_OUT(7)	High Speed Bus Output
97	CLK2_OUT	Clock 2 Output
98	HS_IN(9)	High Speed Bus Input

99	HS_IN(10)	High Speed Bus Input
100	HS_IN(11)	High Speed Bus Input
101	HS_IN(12)	High Speed Bus Input
102	HS_IN(13)	High Speed Bus Input
103	HS_IN(14)	High Speed Bus Input
104	HS_IN(15)	High Speed Bus Input
105	HS_IN(16)	High Speed Bus Input
106	HS_IN(17)	High Speed Bus Input
107	HS_IN(18)	High Speed Bus Input
108	HS_IN(19)	High Speed Bus Input
109	HS_IN(20)	High Speed Bus Input
110	HS_IN(21)	High Speed Bus Input
111	NC	No Connect
112	NC	No Connect
113	HS_IN(22)	High Speed Bus Input
114	NC	No Connect
115	NC	No Connect
116	NC	No Connect
117	HS_OUT28)	High Speed Bus Output
118	HS_IN(32)	High Speed Bus Input
119	HS_OUT(30)	High Speed Bus Output
120	HS_OUT(31)	High Speed Bus Output

Table 1

J4 Connector

Pin	**Pin Name**	**Description**
1	OUT_DATA(3)	Low Speed Output Bus Data
2	HS_OUT(46)	High Speed Bus Output
3	HS_OUT(43)	High Speed Bus Output
4	HS_OUT(45)	High Speed Bus Output
5	HS_OUT(41)	High Speed Bus Output
6	HS_OUT(42)	High Speed Bus Output
7	NC	No Connect
8	HS_OUT(40)	High Speed Bus Output
9	HS_OUT(38)	High Speed Bus Output
10	HS_OUT(39)	High Speed Bus Output
11	IN_DATA(24)	Low Speed Input Bus Data
12	IN_DATA(25)	Low Speed Input Bus Data
13	NC	No Connect
14	NC	No Connect

15	HS_IN(28)	High Speed Bus Input
16	NC	No Connect
17	NC	No Connect
18	HS_OUT(26)	High Speed Bus Output
19	HS_IN(42)	High Speed Bus Input
20	HS_OUT(25)	High Speed Bus Output
21	HS_OUT(27)	High Speed Bus Output
22	HS_IN(35)	High Speed Bus Input
23	HS_OUT(24)	High Speed Bus Output
24	NC	No Connect
25	HS_OUT(44)	High Speed Bus Output
26	NC	No Connect
27	NC	No Connect
28	HS_OUT(37)	High Speed Bus Output
29	NC	No Connect
30	NC	No Connect
31	NC	No Connect
32	NC	No Connect
33	CLK1_OUT	Clock 1 Output
34	HS_OUT(23)	High Speed Bus Output
35	HS_IN(27)	High Speed Bus Input
36	HS_OUT(22)	High Speed Bus Output
37	IN_DATA(26)	Low Speed Input Bus Data
38	IN_DATA(27)	Low Speed Input Bus Data
39	IN_DATA(28)	Low Speed Input Bus Data
40	IN_DATA(29)	Low Speed Input Bus Data
41	FAULT	APP Board Fault Input
42	RD_EN	Low Speed Bus Read Strobe Output
43	ASYNC_RESET_IN	Async reset input
44	COM_GOOD	Communications good output
45	IN_DATA(30)	Low Speed Input Bus Data
46	IN_DATA(31)	Low Speed Input Bus Data
47	HS_IN(0)	High Speed Bus Input
48	HS_IN(1)	High Speed Bus Input
49	HS_IN(2)	High Speed Bus Input
50	HS_IN(3)	High Speed Bus Input
51	HS_IN(4)	High Speed Bus Input
52	HS_IN(5)	High Speed Bus Input
53	HS_IN(6)	High Speed Bus Input
54	HS_IN(7)	High Speed Bus Input
55	HS_OUT(8)	High Speed Bus Output
56	HS_OUT(9)	High Speed Bus Output

57	HS_OUT(10)	High Speed Bus Output
58	HS_OUT(11)	High Speed Bus Output
59	HS_OUT(12)	High Speed Bus Output
60	HS_OUT(13)	High Speed Bus Output
61	HS_OUT(14)	High Speed Bus Output
62	HS_OUT(15)	High Speed Bus Output
63	HS_OUT(16)	High Speed Bus Output
64	HS_OUT(17)	High Speed Bus Output
65	HS_OUT(18)	High Speed Bus Output
66	HS_OUT(19)	High Speed Bus Output
67	IN_DATA(18)	Low Speed Input Bus Data
68	IN_DATA(19)	Low Speed Input Bus Data
69	HS_OUT(20)	High Speed Bus Output
70	HS_OUT(21)	High Speed Bus Output
71	HS_OUT(33)	High Speed Bus Output
72	HS_OUT(29)	High Speed Bus Output
73	OUT_ADDR(0)	Low Speed Output Bus Address
74	OUT_ADDR(1)	Low Speed Output Bus Address
75	OUT_ADDR(2)	Low Speed Output Bus Address
76	OUT_ADDR(3)	Low Speed Output Bus Address
77	OUT_ADDR(4)	Low Speed Output Bus Address
78	OUT_ADDR(5)	Low Speed Output Bus Address
79	HS_IN(24)	High Speed Bus Input
80	HS_IN(25)	High Speed Bus Input
81	OUT_ADDR(6)	Low Speed Output Bus Address
82	OUT_ADDR(7)	Low Speed Output Bus Address
83	OUT_DATA(0)	Low Speed Output Bus Data
84	OUT_DATA(1)	Low Speed Output Bus Data
85	OUT_DATA(2)	Low Speed Output Bus Data
86	HS_OUT(47)	High Speed Bus Output
87	OUT_DATA(4)	Low Speed Output Bus Data
88	OUT_DATA(5)	Low Speed Output Bus Data
89	OUT_DATA(6)	Low Speed Output Bus Data
90	OUT_DATA(7)	Low Speed Output Bus Data
91	IN_DATA(8)	Low Speed Input Bus Data
92	IN_DATA(9)	Low Speed Input Bus Data
93	IN_DATA(10)	Low Speed Input Bus Data
94	IN_DATA(11)	Low Speed Input Bus Data
95	IN_DATA(12)	Low Speed Input Bus Data
96	IN_DATA(13)	Low Speed Input Bus Data
97	IN_DATA(14)	Low Speed Input Bus Data
98	IN_DATA(15)	Low Speed Input Bus Data

99	IN_DATA(16)	Low Speed Input Bus Data
100	IN_DATA(17)	Low Speed Input Bus Data
101	IN_DATA(20)	Low Speed Input Bus Data
102	IN_DATA(21)	Low Speed Input Bus Data
103	HS_OUT(35)	High Speed Bus Output
104	HS_OUT(34)	High Speed Bus Output
105	HS_IN(26)	High Speed Bus Input
106	NC	No Connect
107	NC	No Connect
108	HS_IN(29)	High Speed Bus Input
109	HS_IN(30)	High Speed Bus Input
110	HS_IN(31)	High Speed Bus Input
111	IN_DATA(22)	Low Speed Input Bus Data
112	IN_DATA(23)	Low Speed Input Bus Data
113	NC	No Connect
114	HS_IN(23)	High Speed Bus Input
115	+24VDC	+24VDC Board Power Input
116	+24VDC	+24VDC Board Power Input
117	+24VDC	+24VDC Board Power Input
118	+24VDC	+24VDC Board Power Input
119	+24VDC	+24VDC Board Power Input
120	+24VDC	+24VDC Board Power Input

Table 2

7.2. SAC Board Interface

Figure 5.3.1 shows an isometric rendering of the Rotator Interface Board. Along the back of the board are three connectors that mate with the SAC Board. These connectors are **96 pin DIN** (41612, Type C) 3 rows x 32 pins type connectors. The SAC board provides mates for these connectors and breaks out the signals into D sub and Mil type connectors that provide an interface to both field wiring and to the two Power Modules controlled by the Application board. See [RD4] for more information regarding interface wiring and SAC board connectors.

8. User Interface

A user can interact with the **Instrument Rotator and Cable Chain Interface Module** two ways**.** First the IRCCIM can be controlled and queried by the Rotator software running on the MCSPU.

Second, there are LEDs, Meters and switches on the front panel of the IRCCIM that allow a user to get feedback regarding the status of the Rotators. These indicators are in addition to those found on the front panel of the Power Module.

8.1. Motor Current Display

The front panel of the IRCCIM contains 6 analog meters that will display the current of each of the 6 motors used for a rotator pair. These meters are driven by DACs located on the Applications board. The information regarding the motor current is derived from the CAN bus. The Applications board can query each drive for information regarding the motor current. The Applications board then produces a voltage proportional to this current and drives the front panel meters with this voltage.

A two position switch is located left of the meters. This switch has two positions. In one position the meters display motor current as described above. The second position may be programmed to allow the meters to display an alternate parameter such as bus voltage.

8.2. Application Board Status Display

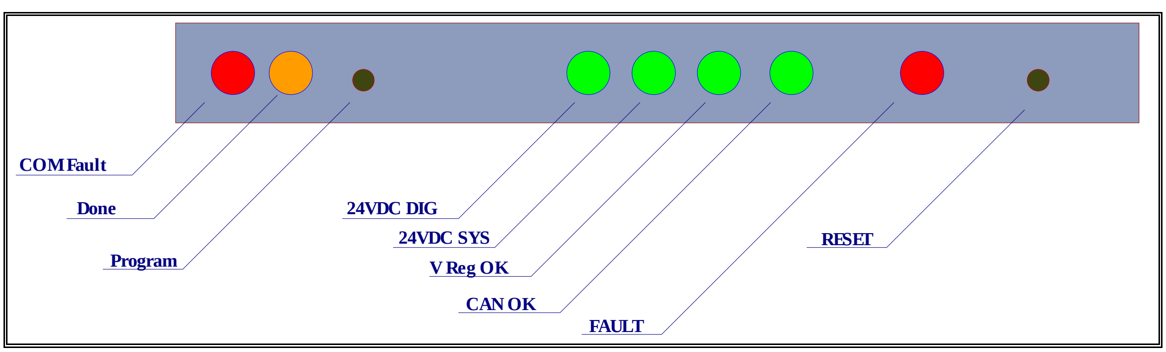

Figure 7.3.1

Figure 7.3.1 shows the LEDs and switches associated with the Rotator Applications Board. Table 7.3.1 provides details about the function of the LEDs, Table 7.3.2 provides details about the function of the push button switches.

COM Fault	This LED indicates a problem with the communications link. Signal is a combination of Rx_Los and the watchdog timer output from the GP Com board
Done	Led is illuminated to indicate that the FPGA on the Aplications Board has been configured correctly.
24VDC DIG	Led is illuminated to indicate that the 24 Volt DC Digital supply is present
24VDC SYS	Led is illuminated to indicate that the 24 Volt DC Digital supply is present.
V Reg OK	This LED is illuminated to indicate that all regulated voltages on the Application board are within spec.
CAN OK	This LED is illuminated to indicate that the CAN bus com is OK
Fault	This LED is illuminated to indicate that the application has detected a fault.

Table 7.3.1

oOo

Doc_info_start
Title: *Instrument Rotator and Cable Chain Interface Module and Operations Manual*
Document Type: *Report*
Source: Steward *Observatory*
Issued by: J. Rosato
Date_of_Issue: *2/16/07*
Revised by:
Date_of_Revision:
Checked by:
Date_of_Check:
Accepted by:
Date_of_Acceptance:
Released by:
Date_of_Release:
File Type: *MS Word*
Local Name:
Category: *675*
Sub-Category: *007*
Assembly: *Instrument Rotator and Cable Chain*
Sub-Assembly:
Part Name:
CAN Designation: *Fill in full doc number here*
Revision: *Preliminary*
Doc_info_end