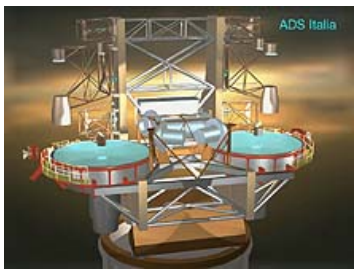

LBT PROJECT
2 x 8.4m TELESCOPE

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LBT PROJECT

2 x 8.4m OPTICAL TELESCOPE

Instrument Rotator and Cable Chain Reef SERDES Interface Module Description and Operations Manual

	Signature	Date
Prepared	J. Rosato	16-Mar-07
Reviewed	D. Ashby	19-Mar-07
Approved		

1. Revision History

Issue	Date	Changes	Responsible
a	16-Mar-07	First draft	J. Rosato

2. Table Of Contents

3. About this document

3.1. Purpose

This document describes the Reef SERDES Interface Module (RSIM). This document is intended as an operator's manual as well as a technical description of the module. This document contains information on configuring the individual channels for proper operation as well as information for debugging problems with the operation of the unit.
A description of how this product is interconnected with the telescope rotator system is also provided.

Technical information such as bill of materials, schematics and printed circuit board layouts for use in maintaining and debugging this product to the component level are listed among the Reference Documents.

3.2. Reference Documents

[RD1] 675s001a – General Purpose SERDES Communications Protocol Standard

[RD2] 675s002a – General Purpose SERDES Communications PC Board Description and Operations Manual

.

[RD3] 483x019a – Datasheet – BittWare Reef Reconfigurable FPGA Board

[RD4] CAN Document XXX.XXX.XXX, Reef Interface Board Schematics

[RD5] CAN Document XXX.XXX.XXX, Reef Module Design Package

[RD6] CAN Document XXX.XXX.XXX, OPJ xxx Reef Interface Board Schematics

3.3. Abbreviations

MCS – Mount Control System
FPGA – Field Programmable Gate Array
SERDES – Serializer - Deserializer
CRC - Cyclic Redundancy Check
VHDL- Very High Speed Integrated Circuit Hardware Description Language
GPSCOM- General Purpose Communications
DGR- Direct Gregorian Rotator
FBGR - Front Bent Gregorian Rotator
CBGR- Center Bent Gregorian Rotator
RBGR- Rear Bent Gregorian Rotator

4. Overview of Operation

The Reef SERDES Interface Module (RSIM) provides a high speed serial interface between the Bitware Reef board located in the MCS control chassis and up to four GPSCOM modules. The Reef Serial Interface Module contains four Reef Interface boards each capable of controlling 2 axis of rotator motion (left and right sides)

The Reef SERDES Interface Module connects to the Reef board [RD3] through a 68 pin SCSII type connector on the front to the Reef board. The signals on this connector are routed to the Xilinx Virtex II FPGA on the Reef board. Custom VHDL code provides the logic to serialize all I/O needed for the LBTO rotators. Connection to the GPCOM module is through a multi mode fiber optic cable. See [RD1] and [RD2] for details on serial interface.

Figure 1 below shows the interconnects for a RSIM controlling 4 rotators.

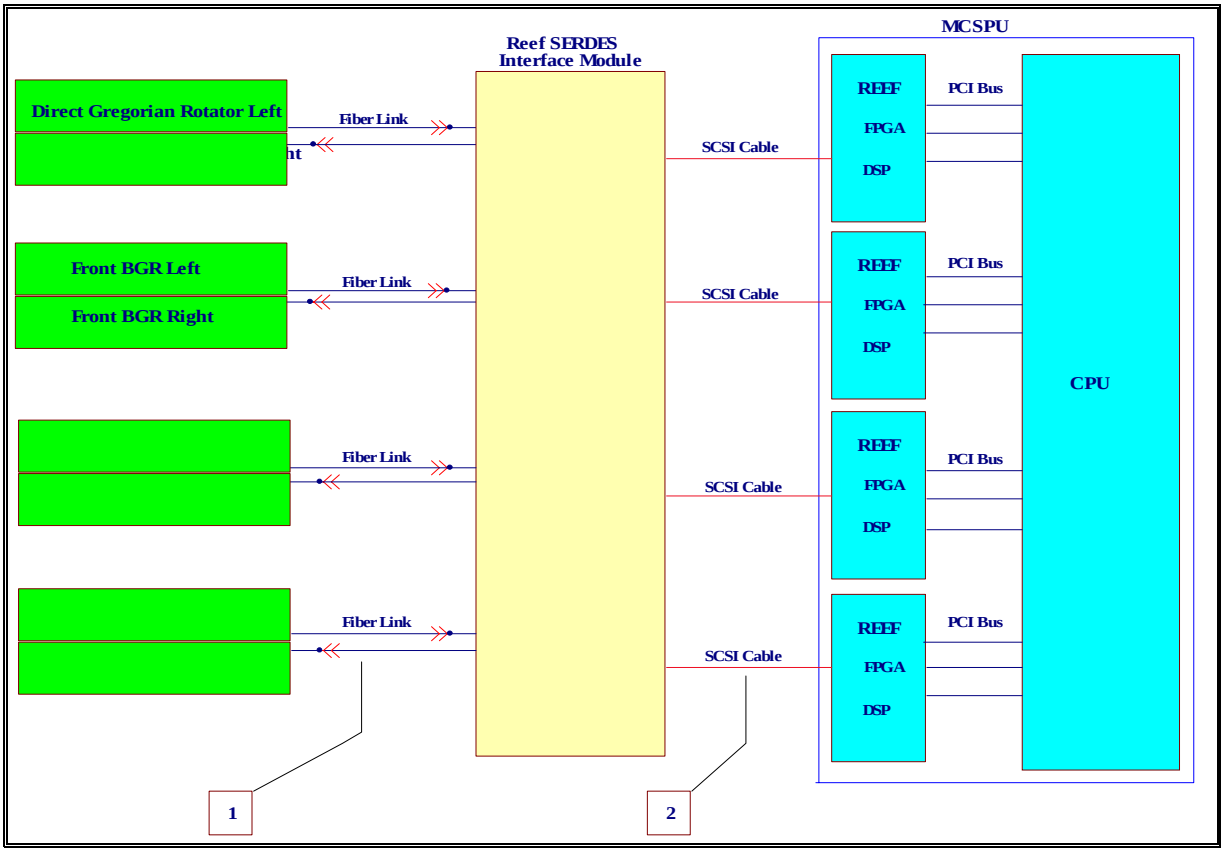


Figure 4.0.1: This block diagram shows the use of the Reef SERDES Interface Module in the LBT rotator control system. The Reef Interface Board connects to the Reef boards located in the MCS rack through a standard 68 pin SCSI type cable.

	Cable Designator	**Description**
1	DGFC1	Direct Gregorian Fiber Cable 1
1	FLBGFC1	Front Left Bent Gregorian Fiber Cable 1
1	FCBGFC1	Front Center Bent Gregorian Fiber Cable 1
1	FRBGFC1	Front Right Bent Gregorian Fiber Cable 1
2	DGDC1	Direct Gregorian Data Cable 1
2	FLBGDC1	Front Left Bent Gregorian Data Cable 1
2	FCBGDC1	Front Center Bent Gregorian Data Cable 1
2	FRBGDC1	Front Right Bent Gregorian Fiber Cable 1

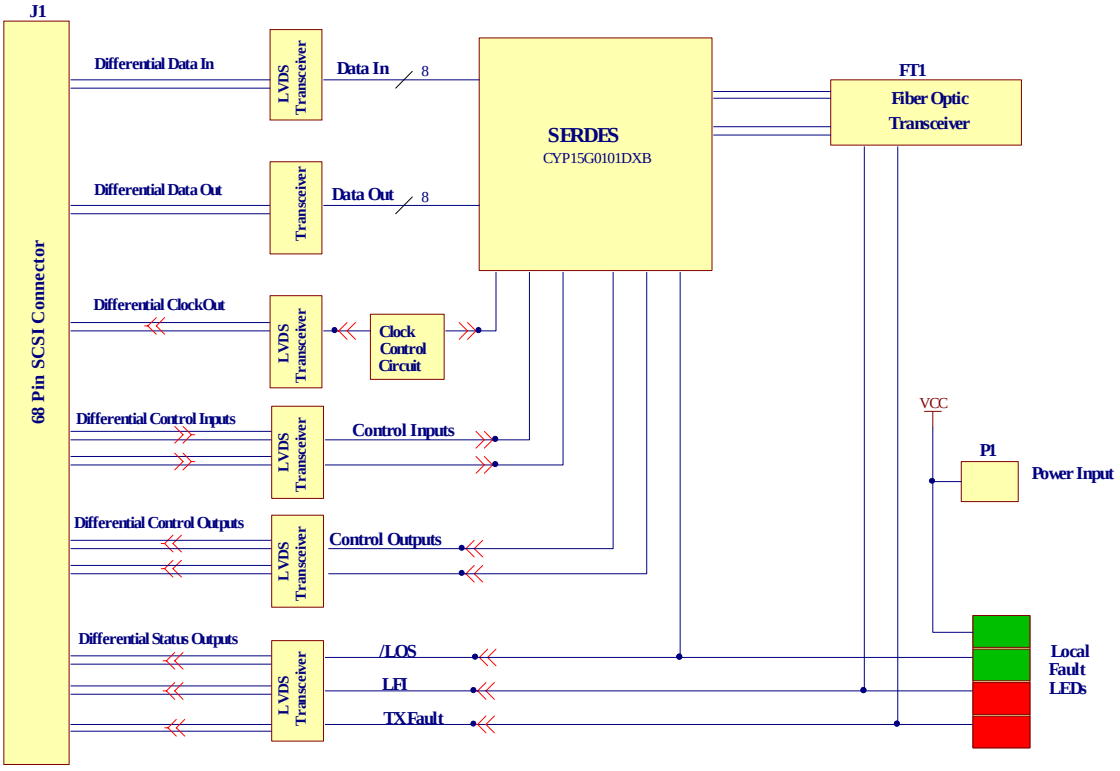
Table 4.0.1

5. Reef Interface Printed Circuit Board

The Reef Interface Board is the heart of the Reef Serial Interface Module (RSIM). The RSIM can contain up to 4 Reef Interface Boards allowing control of 4 different pairs of rotator axis (Left and Right)

5.1. Block Diagram

The block diagram below illustrates the functions of the Reef Interface Board.



J1 connects signals from the Reef board to the Reef Interface Board.
P1 connects external power to the voltage regulation circuitry on the board.
FT1 provides a fiber optic interface from the Reef Interface Board to the GP Com board.

The RIB provides nine major functions

1. Provides the physical interface between the Reef board and the Reef interface Board. This interface is LVDS and provides for both receiving and transmitting data from the RIB .
2. Provides a method to move 8 bits of parallel data from the Reef FPGA to the SERDES on the RIB.
3. Provides a method to move 8 bits of parallel data from the SERDES on the RIB to the Reef FPGA.
4. Provides a Clock source for both the SERDES and the FPGA on the Reef Board.
5. Provides an input control bus to allow the FPGA on the Reef board to control the SERDES
6. Provides an output control bus to allow the SERDES on the RIB to provide control information to the FPGA on the Reef board.
7. Provides status bits to allow the FPGA on the Reef board to monitor critical signals from the SERDES the Fiber optic transceiver.
8. Provides LEDs for local monitoring of critical signals from the SerDes and the Fiber optic transceiver.
9. Provides voltage regulation and power monitoring.

See [RD4] for schematics.

6. Mechanical Packaging and Environment

6.1. Environmental Specifications

Temp	0º to +50 ºC
Humidity	0 to 90% non condensing
Ventilation requirements	Unit must be mounted so that internal fans can draw air from the front of the module and exhaust air out the back
Distance from Reef Board	1Meter Max
Power Input	5 Volt ±5%
	5 Amps Max

6.2. Mountain Location

When used for the LBT Rotator Control System the RSIM is located in the Aux Control room in a 1 U, 19 inch rack space directly over the MCSPU. The RSIM is connected to up to four Reef interfaces in the MCSPU by 1Meter standard SCSI cables. Because of the speed of signals and delay in transmission of critical clock signals, the length of the cables connecting the Reef board to the RSIM module should be 1 Meter or less. The delay due to the length of this cable is compensated on the Reef Interface board by setting jumpers that control the ROBOCLOCK circuit. See table 7.2.2 for more details.

6.3. Mechanical Drawings

Figure 6.3.1: The RSIM is housed in a 1U standard enclosure shown below.

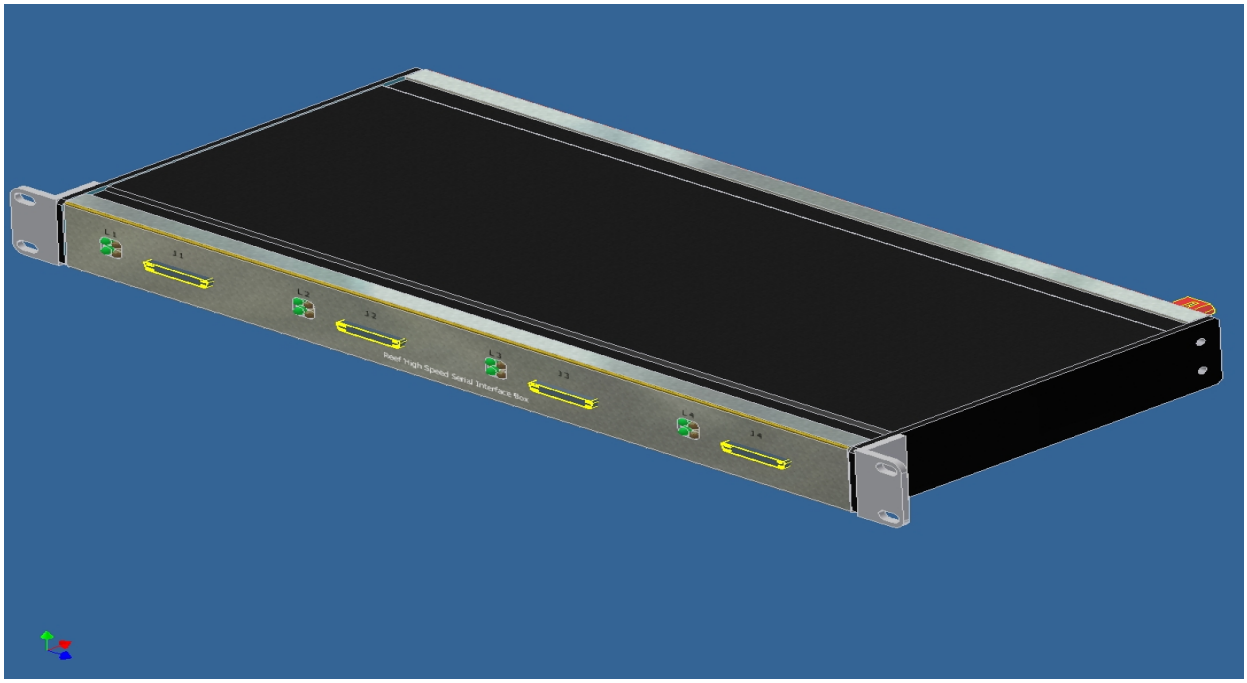


Figure 6.3.2: Front panel of the RSIM

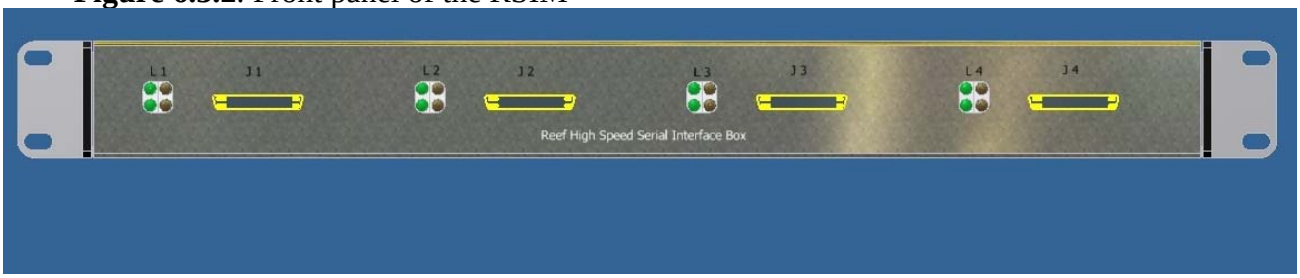


Figure **6.3.3**: Rear Panel of the RSIM

7. Input and Output Specifications

7.1. List of Signals and Their Connectors

The RSIM has the following interconnects.

Connector	Description	I/O standard	Location
J1	68 pin female SCSI connectors	LVDS	Front
J2	68 pin female SCSI connectors	LVDS	Front
J3	68 pin female SCSI connectors	LVDS	Front
J4	68 pin female SCSI connectors	LVDS	Front
J5	3-Pin power connector	+5Volt ±5% 5 Amps	Rear
FT1	IEEE 802.3 Gigabit Ethernet Fiber optic transceiver	LC Duplex Optical	Rear
FT2	IEEE 802.3 Gigabit Ethernet Fiber optic transceiver	LC Duplex Optical	Rear
FT3	IEEE 802.3 Gigabit Ethernet Fiber optic transceiver	LC Duplex Optical	Rear
FT4	IEEE 802.3 Gigabit Ethernet Fiber optic transceiver	LC Duplex Optical	Rear

Front view of Connectors with Signal Definitions

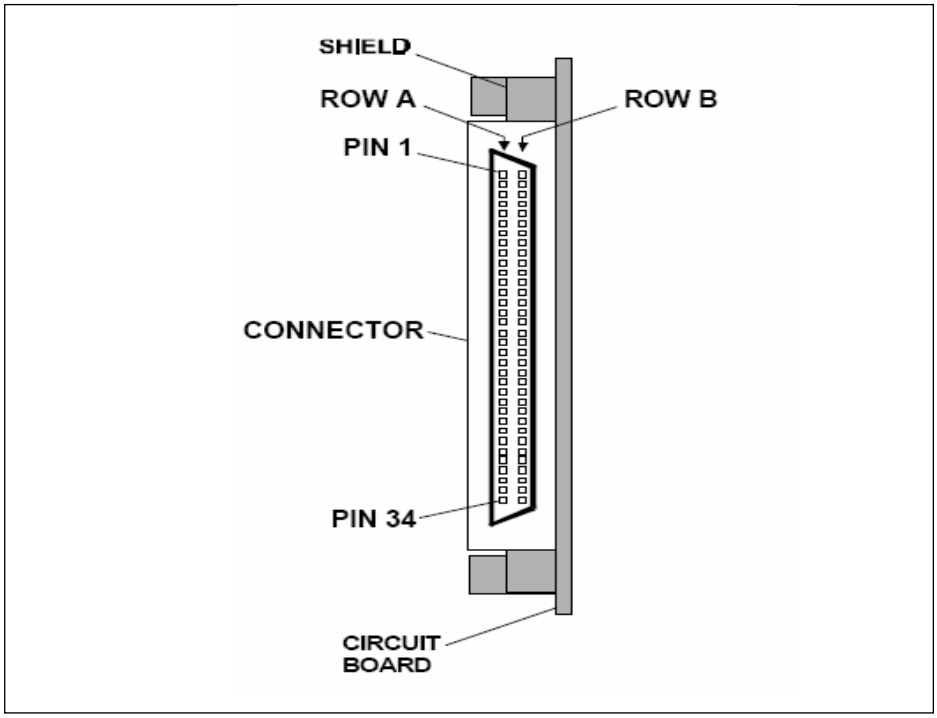


Figure 7.1.1

Table 7.1.1: The I/O Connector Pin out for the 68 Pin SCSI type connector on the front of each Reef interface board. Is detailed below.

Reef Connector Pin Number	**Reef board Name**	**Reef interface Board Name**	**I/O**
1	GND/xexep_n1		
35	GND/ xexep_p1	GND	Power
2	xexep_n2		
36	xexep_p2	SCSEL	Out
3	xexep_n3		
37	xexep_p3	TXCT0	Out
4	xexep_n4		
38	xexep_p4	TXCT1	Out
5	xexep_n5		
39	xexep_p5	TRSTZ/	Out
6	xexep_n6		
40	xexep_p6	TXD7	Out
7	xexep_n7		
41	xexep_p7	TXD6	Out
8	xexep_n8		
42	xexep_p8	TXD5	Out
9	xexep_n9		
43	xexep_p9	TXD4	Out
10	xexep_n10		
44	xexep_p10	TXD3	Out
11	xexep_n11		
45	xexep_p11	TXD2	Out
12	xexep_n12		
46	xexep_p12	TXD1	Out
13	xexep_n13	TXD0	
47	xexep_p13		Out
14	xexep_n14	N.C	
48	xexep_p14		

Reef Connector Pin Number	Reef board Name	Reef interface Board Name	I/O
15	xexep_n15		
49	xexep_p15	DCM_CLKO	Out
16	xexep_n16		
50	xexep_p16	TXRST/	Out
17	xexep_n17		
51	xexep_p17	RXST1	In
18	xexep_n18		
52	xexep_p18	RXST2	In
19	xexep_n19		
53	xexep_p19	RXST0	In
20	xexep_n20		
54	xexep_p20	DCM_CLKI	In
21	xexep_n21		
55	xexep_p21	RXD6	In
22	xexep_n22		
56	xexep_p22	RXD7	In
23	xexep_n23		
57	xexep_p23	RXD5	In
24	xexep_n24		
58	xexep_p24	RXD4	In
25	xexep_n25		
59	xexep_p25	CLKIN	In
26	xexep_n26		
60	xexep_p26	RXD2	In
27	xexep_n27		
61	xexep_p27	RXD3	In
28	xexep_n28		
62	xexep_p28	RXD1	In

Reef Connector Pin Number	Reef board Name	Reef interface Board Name	I/O
29	xexep_n29		
63	xexep_p29	RXD0	In
30	xexep_n30		
64	xexep_p30	LFI	In
31	xexep_n31		
65	xexep_p31	RX_Loss	In
32	xexep_n32		
66	xexep_p32	TX_Fault	In
33	xexep_n33		
67	xexep_p33	PWR_OK	In
34	xexep_n34		
68	xexep_p34	GND	Power

7.2. Rear View of Connectors with Signal Definitions

Figure 7.2.1

FT1 through FT4 are Small Form Factor Pluggable (SFP), Multi-Source Agreement complaint, 1.25Gb fiber transceivers. Using pluggable transceivers allows the transceivers to not only have multiple sources, but to be replaced in the field in case of failure. Additionally, this approach allows transceivers implementing different protocols and speeds, to be supported by the same board layout. Figure 6.3.2 is an illustration of this component with the transmit and receive ports identified.

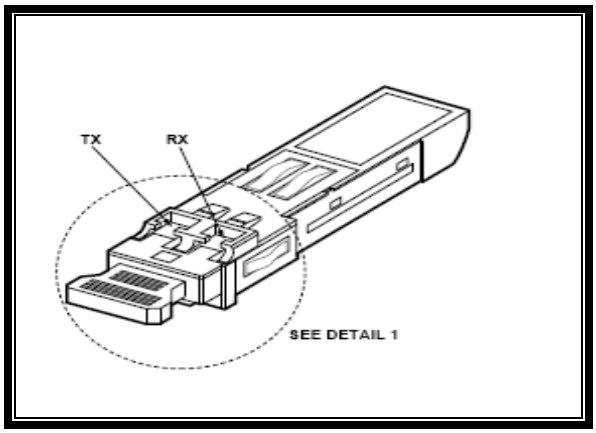


Figure 7.2.2

The FT numbers on the rear of the RSIM are associated with the J numbers on the front of the module. That is signals entering J1 are serialized and exit on FT1.

Fiber Transceiver Details: Table 7.2.1

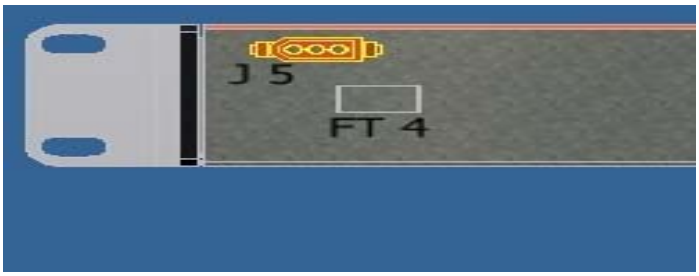
IEEE 802.3 Gigabit Ethernet (1.25GBd) 1000BASE-SX compliant	
Small Form Factor Pluggable (SFP)Multi-Source Agreement (MSA) compliant	
Hot-pluggable	
+3.3 V DC power supply	
850 nm Vertical Cavity Surface Emitting Laser (VCSEL)	
LC-Duplex fiber connector compatible	
Fiber compatibility:	**– 2 to 550 meters with 50/125 μm fiber** **– 2 to 275 meters with 62.5/125 μm fiber**
Eye safety certified:	**– US 21 CFR(J)** **– EN 60825-1 (+All)**

For detailed information regarding this module see [RD5]

Power is provided to the module through J5. The table below gives details of J5 signals.

Table 7.2.2

Pin Number	Description
1	+5 Volts
2	Return
3	+5 V sense



8. User Interface

The user interface on the RSIM consists of LEDs to indicate unit status and jumper and switch settings on the board that control various functions.

8.1. LED Indicators and their functions

Each Reef Interface Board in the module contains a four LED block to indicate the status of the board.

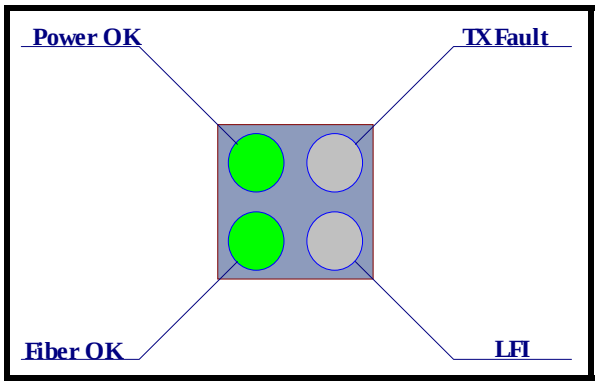


Figure 8.1.1: LED block

During normal operation the Power OK and Fiber OK LEDs will be green and the TX Fault and LFI LEDs will be off.

The table below details the function of each LED.

Power OK:	This LED will be on (green) when there is power supplied to the Reef Interface Board.
Fiber OK:	This LED will be on (green) when the fiber optic transceiver detects an adequate signal to operate properly.
TX Fault	**Transmitter Fault Indicator:** This LED will be on (Red) when the fiber transceiver detects a laser fault of some kind.
LFI	**LFI- Link Fault Indication:** This LED will be illuminated (Red) to indicate one of four errors detected by the SerDes chip. These error are: • Received serial data frequency outside of expected range • Analog amplitude below expected levels • Transition density lower than expected • Receive channel disabled

For information on using these indictors to debug problems with the Reef Serial Interface Module, see section 9.0 .

8.2. Jumper and Dip-Switch functions

Table 8.2.1 gives a detailed description of all the control pins in J1.

Many of the static control signals are of 3-level select. This means that they operate at three voltage levels, which are termed as
• HIGH (Direct connection to Vcc)
• MID (Open or allowed to float)
• LOW (Direct connection to Vss, i.e., GND).

In J1 these levels are implemented as follows:

• HIGH – Place a shunt across columns 1 and 2
• MID – Don't place any shunt
• LOW – Place a shunt across columns 2 and 3.

Table 8.2.1

Pin Name	Characteristions
TXMODE0, TXMODE1	Transmit mode (two inputs) 3-Level Select • Configure LL for Encoder bypass • LM and LH are reserved for testing (we will be using LM in our tests) • All other combinations along with the selection of SCSEL are for encoder control. (Please refer to the data sheet for more details.)
TXCKSEL	Transmit Clock Select (1 input) 3-Level Select • When L, REFCLK is used by all the input registers. • When M or H, TXCLK is used.
SPDSEL	Serial Rate Select 3-level select • LOW = 195–400 MBd • MID = 400–800 MBd • HIGH = 800–1500 MBd
SDASEL	Signal Detect Amplitude Level Select 3-Level Select • LOW = 140 mV peak-peak differential • MID = 280 mV peak-peak differential • HIGH = 420 mV peak-peak differential
PARCTL	Parity check/generate control 3-Level Select • LOW = Parity checking is disabled • MID = If encoder/decoder is enabled, inputs are checked for odd parity • HIGH = If encoder/decoder is enabled, inputs are checked for odd parity
RXMODE	Receive Operating Mode. This input selects one of two RXST channel status reporting modes. • L: Status A selected

	• M: Reserved for Test • H: Status B selected This input is interpreted only when DECMODE is not LOW.
RXCKSEL	Receive Clock Mode. 3-Level Select • L: Output register is clocked by REFCLK. — RXCLK± presents a buffered/delayed form of REFCLK. • M: Output register is clocked by the recovered clock. — RXCLK+ follows the recovered clock as selected by RXRATE. — The elasticity buffer is bypassed. • H: Invalid State.
RFMODE	Reframe Mode Select. 3-Level Select Please refer to the data sheet for CYP15G0101DXB for detailed information.
FRAMCHAR	Framing Character Select. 3-Level select. Please refer to the data sheet for CYP15G0101DXB for detailed information.
DECMODE	Decoder Mode Select. 3-Level Select • L: Decoder bypassed • M: Cypress decoder table for special code characters is used. • H: Alternate decoder table for special code characters is used.

Jumpers JP4 through JP14 are used to configure the ROBOCLOCK IC on the Reef Interface Board. These jumpers allow the edge of the clock signal sent to the Reef board to be adjusted to compensate for the length of the SCSI interconnect cable.

Table 8.2.2 details the default settings for the 1 meter cable specified for the Rotator system .

Table 8.2.2

JP4	JP5	JP6	JP7	JP8	JP9	JP10	JP11	JP12	JP13	JP14
Open	**Open**	**Open**	**Open**	**Open**	**Open**	2-3	**Open**	**Open**	**Open**	**Open**

See [RD5] for details on the ROBOCLOCL operation.

Dip Switch Settings

The Reef Interface Boards have a 12 position dip switch (SW1) that can be used to configure various options available from the SERDES chip. *Table 7.2.2* describes these various functions, as well as their default positions.

Table 8.2.3

Switch Number	Signal name	Description	Default
1	LPEN	All-Channel Loop-Back-Enable. LVTTL Input Active HIGH. When HIGH • Transmit serial data is internally routed to receive serial data • All external serial data inputs are ignored When LOW, the transmit data is not looped back to the receive side.	Off
2	RFEN	LVTTL Input Active HIGH. When HIGH • Transmit serial data is internally routed to receive serial data • All external serial data inputs are ignored When LOW, the transmit data is not looped back to the receive side. Reframe Enable for all channels. Active HIGH.	On
3	RXRATE	Receive Clock Rate Select. 2-Level Select LVTTL Input • L: RXCLK+ operates at the recovered channel clock rate • H: RXCLK+ operates at HALF the recovered channel clock rate	On
4	TXCLK		On
5	TXRATE	LVTTL Input • When H, the transmit PLL multiplies REFCLK by 20 to generate the bit rate clock. • When L, the transmit PLL multiplies REFCLK by 10 to generate the bit rate clock.	On
6		Not Used	N/A
7	INSEL	Receive Input Channel Selector. LVTTL Input. • HIGH - IN1± input is passed into the CDR circuit • LOW - IN2± input is passed into the CDR circuit For example, if INSEL is selected as HIGH, IN1± input will be passed into the receiver.	On
8	BISTLE	(Transmit and Receive BIST Latch Enable) • Active HIGH	On
9	OELE	OELE (Serial output driver enable latch enable) • Active HIGH	On
10	RXLE	(Receive channel enable latch enable) • Active HIGH	On
11	BOE0	• BIST, serial output, and receive channel enables. • LVTTL Input	On

12	BOE1	• BIST, serial output, and receive channel enables. • LVTTL Input	On

9. Debugging RSIM problems

The Maintenance philosophy for the RSIM is that it is considered a field replaceable module. That is spares for this module should be keep on hand and if a problem is detected with this unit, it can be swapped out with a spare.

This is done easily by

1. Remove 5 volt power by disconnecting J5 from the back of the box.
2. Remove any fibers plugged into FT1 through FT4 on the rear of the

The table 9.0.1 below gives some suggested options for debugging and repairing the RSIM.

Table 9.0.1

Symptom	**Repair options**
Power OK LED is not illuminated	• Check power to the unit • If other RIBs in module show power ok, check internal power connections, and or fuses on RIB
Fiber OK LED is not Illuminated	• Check that fiber is connected or that fiber is not broken • Check that the transmitter on the other end of the fiber connection is enabled. • Replace the Fiber Optic Module
Tx Fault LED is illuminated	• Replace the Fiber Optic Module
LFI LED is illuminated	• Check that the cable between the Reef board and the RSIM is connected correctly • Insure that the FPGA on the attached Reef board is programmed and running. • Check that the Reef Interface Board has clock option jumpers set correctly.

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CAN Designation: *657s003*
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Doc_info_end