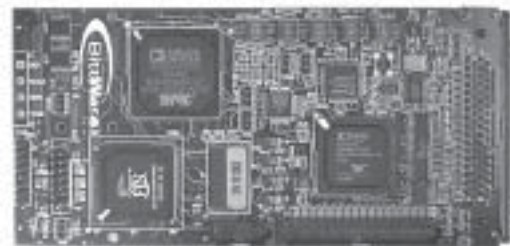


# Reef-PMC+

## Reconfigurable FPGA Board



### Flexible Application Design with ADSP-21160 Processing Power

BittWare's Reef-PMC+ (RFPM) is a reconfigurable FPGA board combining the power of the XILINX Virtex-II FPGA and the Analog Devices ADSP-21160 SHARC® DSP. Configurable for nearly any application, the RFPM allows system designers to take advantage of both the flexibility of a reconfigurable FPGA and the processing power of a general-purpose DSP. The Virtex-II features up to 1 million system gates, a flexible digital I/O interface, and reconfigurable computing blocks. And the ADSP-21160 DSP provides additional I/O and processing power for the board. Rounding out the RFPM's feature set are a 64/66 PCI interface, a 64-512 MB bank of SDRAM, and 2 MB of Flash memory.

### XILINX Virtex-II Reconfigurable FPGA

The Virtex-II reconfigurable FPGA from XILINX is a powerful tool for designing custom digital interfaces based on IP cores and customized modules. The RFPM features a flexible digital I/O interface that provides up to 140 user I/O pins, each of which is individually configurable for any of nineteen single-ended I/O standards and six differential I/O standards, including LVDS, SSTL, HSTL II, and GTL+. Any two I/O pins can be used as a differential pair, providing maximum board layout flexibility. The Virtex-II is configured on power-up by the host or an on-board EPROM, and it supports reconfiguration "on-the-fly" from either the host or the ADSP-21160 DSP.

### BittWare's SharcFIN ASIC

The SharcFIN ASIC provides a full 64-bit 66 MHz master PCI interface, flexibly interfaces the ADSP-21160 to peripherals such as the Flash, and implements an extensive flag and interrupt multiplexer. It also provides a full-featured SDRAM controller to interface the SDRAM to the DSP, the Virtex-II, and the PCI host.

### I/O Options

The Virtex-II can send and receive data via the SharcFIN, which provides the 64/66 PCI interface, or via a high-density 68-pin I/O connector on the front panel. The Virtex-II also supports two link ports and a serial port that connect it directly to the ADSP-21160, allowing the DSP to move data between the Virtex-II and the host via the PMC+ interface. A local parallel bus gives the Virtex-II high-speed access to the SDRAM, the SharcFIN, and the ADSP-21160.

In addition to the 68-pin front panel I/O connector, two optional I/O connectors are also available. One provides 68 pins of I/O, and the other provides 4 pins of I/O for a total of 140 user I/O pins. Both 68-pin connectors are available with optional LVDS input terminations, either 34 pairs or 17 pairs.

### Available Development Tools

BittWare offers complete software development tools that allow designers to easily develop application code and integrate the RFPM into their systems. XILINX also provides a complete suite of development tools for the Virtex-II. Please note that the end user is responsible for generating, assembling, and debugging all application-specific FPGA design for the Virtex-II; however, custom FPGA design is also available from BittWare.

## Features

- XILINX Virtex-II Reconfigurable FPGA (XC2V1000)
- Reconfigurable digital I/O (up to 140 user I/Os)
- Supports single-ended or differential signaling
- Reconfigurable computing blocks
- 1 million system gates
- On-the-fly reconfiguration
- 80 MHz Analog Devices ADSP-21160 SHARC DSP
- 64-512 MB of SDRAM
- BittWare SharcFIN ASIC
- 64-bit, 66 MHz PCI interface (Rev. 2.2 compliant)
- 2 MB of Flash memory for boot loading
- PMC interface with BittWare's PMC+ extensions (external link and serial ports)
- Complete software development tools available for both the Virtex-II and the ADSP-21160



# Reef-PMC+ Specifications

## BOARD ARCHITECTURE

### XILINX Virtex-II FPGA (XC2V1000)

- 1 million system gates
- Up to 140 user-accessible I/Os, depending on connectors installed (68 + 68 + 4)
- Supports 19 single-ended standards and 6 differential standards
- SRAM-based in-system configuration via EPROM or host

### XILINX I/O Options

- Two link ports and a serial port from Virtex-II to ADSP-21160
- Local parallel bus with high-speed access to SDRAM, SharcFIN ASIC, and ADSP-21160
- 68-pin high-density (SCSI-II type) connector for I/O to/from Virtex-II (connector A)
- Optional LVDS input terminations available
- 32 pins of connector A are 5 volt tolerant
- Optional 68-pin (connector B) and 4-pin (connector C) I/O connectors (require second slot; violates PMC single slot spec.)

### JTAG Interface

- Optional JTAG connectors for in-circuit emulation of ADSP-21160 and configuring of Virtex-II

### ADSP-21160 DSP

- 80 MHz Analog Devices ADSP-21160 SHARC DSP
- 4 Mb of on-chip dual-ported SRAM
- Integrated I/O processor with fourteen-

channel DMA controller, six 80 Mbyte/sec link ports, and two 40 Mbit/sec serial ports

- PMC+ extensions provide four link ports and a TDM serial bus directly to ADSP-21160

### SharcFIN™ ASIC

- 64/66 MHz PCI rev. 2.2 compliant interface (528 burst)
- SDRAM controller on SHARC bus; supports up to 512 MB
- SDRAM mapped into PCI memory space
- Supports host- and Flash-based booting of ADSP-21160

### On-Board Memory

- 64-512 MB SDRAM (standard 144-pin SODIMM)
- 2 MB Flash memory for hostless boot or non-volatile storage

### Power

- 10W @ 3.3V worst case; 3 A max current
- 0.5W @ 5V worst case; 100 mA max current

### Size

- 74mm x 149mm PMC form factor

## SOFTWARE SUPPORT

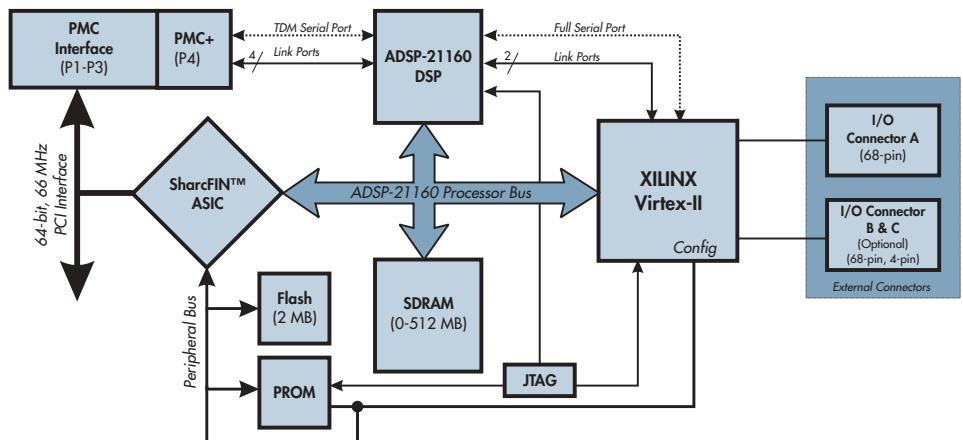
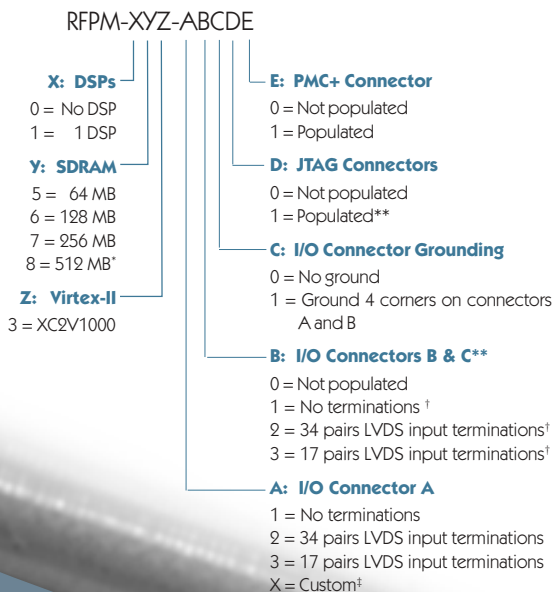
### Host Interface

- BittWare's software development kit for Windows® 95/98/NT/2000 and Linux contains a C-callable library of board control and communications routines
- Porting kit available for other operating system platforms

### Development Tools

- Analog Devices' VisualDSP tools: C compiler, assembler, linker, simulator, and debugger
- VisualDSP Target for on-board ADSP-21160 debugging from host without an ICE
- Analog Devices ICE emulators\*
- BittWare SharcLAB interface to MATLAB, Simulink®, Stateflow®, and Real-Time Workshop®
- BittWare SpeedDSP ADSP-21xxx optimized function libraries
- XILINX Multilink cable support\*\*

## Ordering Information



\*\* Requires optional JTAG connectors

\* Currently unavailable  
\*\* Violates PMC height spec for single slot  
† Connector B only  
‡ Contact BittWare

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